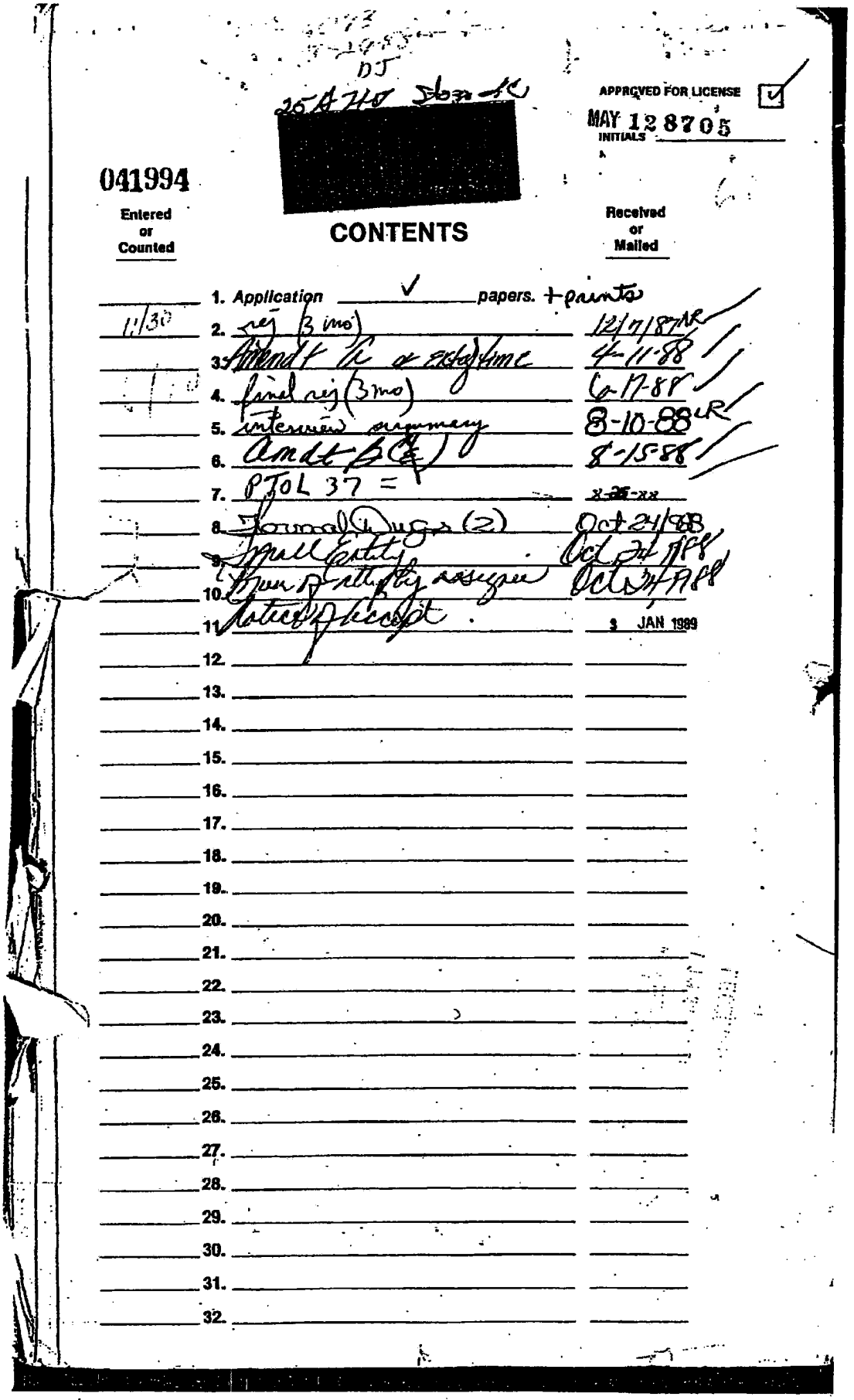
DX 102



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INITIALS

041994

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CONTENTS

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	1.	Application ✓ papers. + prints	
11/30	2.	rej (3 mo)	12/7/87 AR
	3.	Amdt & Rem & extn time	4-11-88
	4.	final rej (3 mo)	6-17-88
	5.	interview summary	8-10-88 AR
	6.	Amdt B (2)	8-15-88
	7.	PTOL 37 =	8-25-88
	8.	Issue Fee (2)	Oct 24 1988
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	11.	Notice of Allowance	9 JAN 1989
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Case No. 04-1371-JJF
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Signature _____

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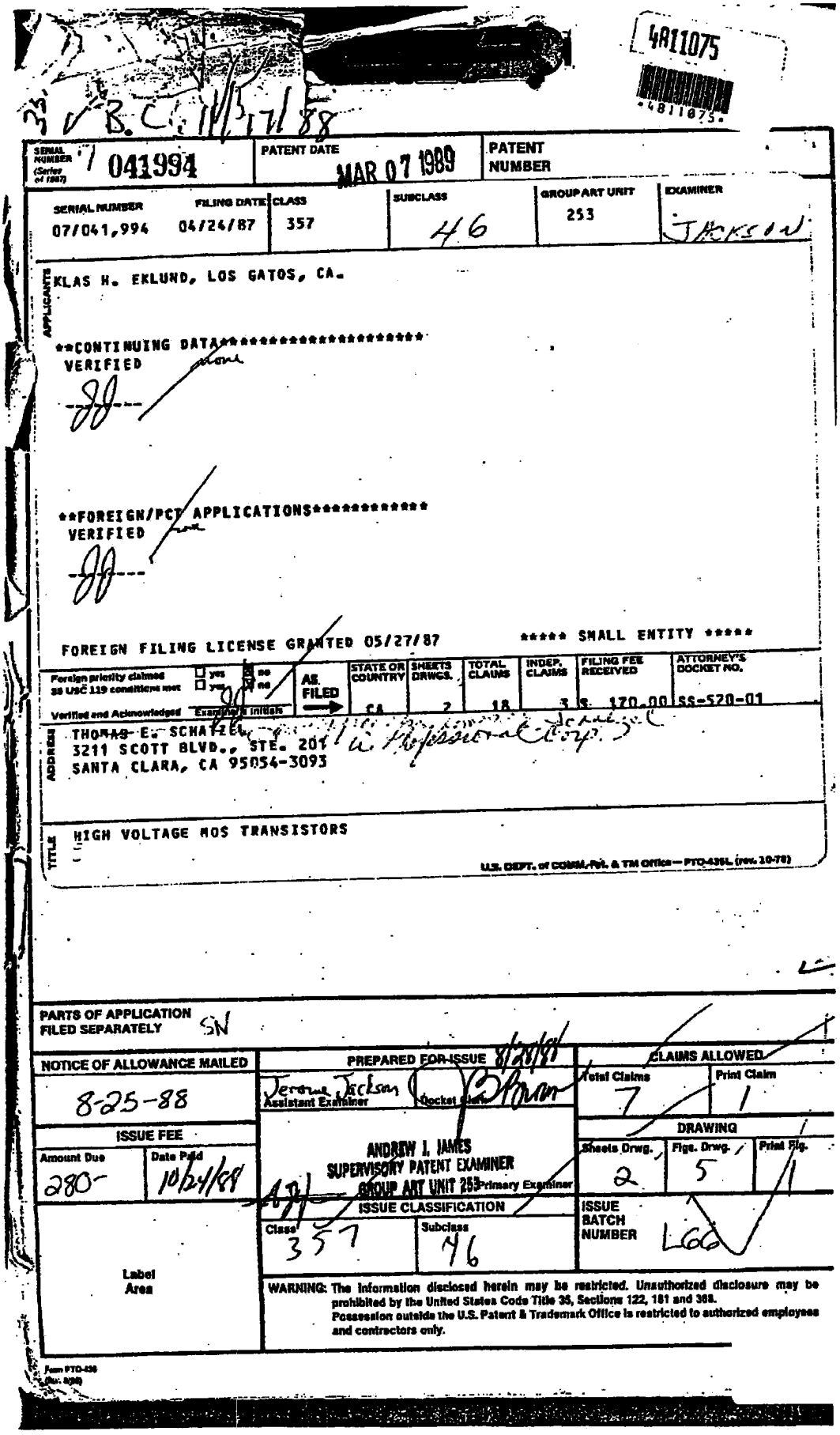

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35 U.S.C. 11/3/17/88

SERIAL NUMBER (Series of 1987)	PATENT DATE	PATENT NUMBER
041994	MAR 07 1989	

SERIAL NUMBER	FILING DATE	CLASS	SUBCLASS	GROUP ART UNIT	EXAMINER
07/041,994	04/24/87	357	46	253	JACKSON

APPLICANTS: KLAS H. EKLUND, LOS GATOS, CA.

CONTINUING DATA********
VERIFIED

FOREIGN/PCT APPLICATIONS********
VERIFIED

FOREIGN FILING LICENSE GRANTED 05/27/87 ***** SMALL ENTITY *****

Foreign priority claimed 35 USC 119 conditions met	Verified and Acknowledged	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDEP. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
☐ yes ☐ no / ☐ yes ☐ no	Examiner's Initials		CA	2	18	3	$ 170.00	SS-520-01

ADDRESS: THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

TITLE: HIGH VOLTAGE MOS TRANSISTORS

U.S. DEPT. of COMM./Pat. & TM Office — PTO-436L (rev. 10-78)

PARTS OF APPLICATION FILED SEPARATELY SN

NOTICE OF ALLOWANCE MAILED	PREPARED FOR ISSUE	CLAIMS ALLOWED
8-25-88	8/26/88	Total Claims: 7 / Print Claim: 1

Jerome Jackson, Assistant Examiner — Docket Clerk

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253
Primary Examiner

ISSUE FEE		DRAWING		
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.	Print Fig.
280-	10/24/88	2	5	1

ISSUE CLASSIFICATION		ISSUE BATCH NUMBER
Class	Subclass	
357	46	L66

Label Area

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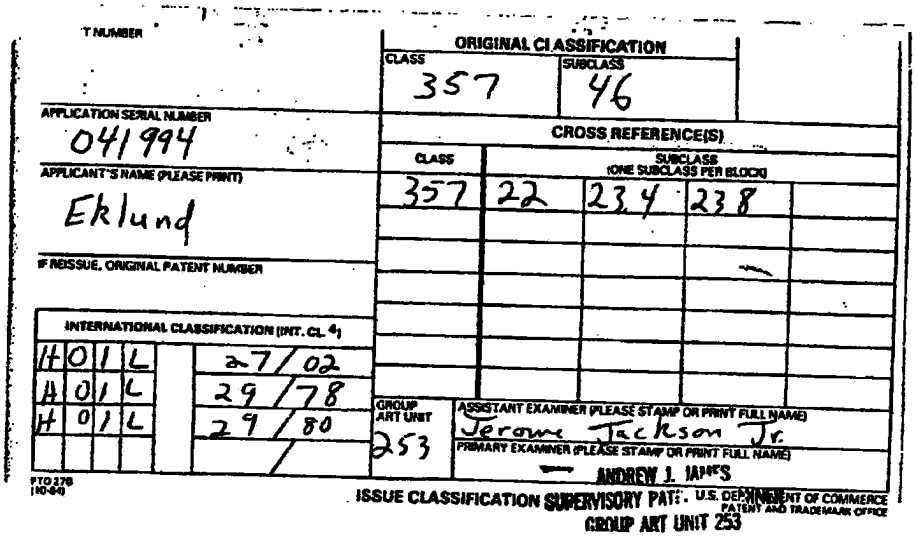
Form PTO-436 (Rev. 8/88)



T NUMBER

ORIGINAL CLASSIFICATION
CLASS 357 SUBCLASS 46

APPLICATION SERIAL NUMBER
041994

APPLICANT'S NAME (PLEASE PRINT)
Eklund

IF REISSUE, ORIGINAL PATENT NUMBER

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
357	22	234	238	

INTERNATIONAL CLASSIFICATION (INT. CL. 4)

H	01	L	27/02
H	01	L	29/78
H	01	L	29/80
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GROUP ART UNIT 253

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
Jerome Jackson Jr.

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
ANDREW J. JAMES

PTO 270
(10-83)

ISSUE CLASSIFICATION SUPERVISORY PAT.

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

GROUP ART UNIT 253

FORM PTO-875 (REV. 1-86) — U.S. DEPARTMENT OF COMMERCE, PATENT AND TRADEMARK OFFICE

PATENT APPLICATION FEE DETERMINATION RECORD

SERIAL NO. 041994 — FILING DATE April 24, 1987

APPLICANT (FIRST NAMED) Klaus H. Eklund

CLAIMS AS FILED - PART I

FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
TOTAL CLAIMS	18 -20=	* 0
INDEP. CLAIMS	3 -3=	* 0
☐ MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in col. 1 is less than zero, enter "0" in col. 2

SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY FEE
	$170	OR		$340
x6=	$	OR	x12=	$
x17=	$	OR	x34=	$
x56=	$	OR	x110=	$
TOTAL	$170	OR	TOTAL	$

CLAIMS AS AMENDED - PART II

	(1) CLAIMS REMAINING AFTER AMENDMENT		(2) HIGHEST NO. PREVIOUSLY PAID FOR	(3) PRESENT EXTRA
AMENDMENT A — TOTAL	* 17	MINUS	** 20	=
AMENDMENT A — INDEP.	* 2	MINUS	*** 3	=
AMENDMENT A — ☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				
AMENDMENT B — TOTAL	* 17	MINUS	** 20	=
AMENDMENT B — INDEP.	* 2	MINUS	*** 3	=
AMENDMENT B — ☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				
AMENDMENT C — TOTAL	*	MINUS	**	=
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AMENDMENT C — ☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

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x15=	$	OR	x30=	$
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+50=	$	OR	+100=	$
TOTAL ADDIT. FEE	$	OR	TOTAL	$

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.

** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest No. Previously Paid For" (Total or Indep.) is the highest number found in the appropriate box in Col. 1.

PTO-1139 (Rev. 2-93) U.S. DEPARTMENT OF COMMERCE-PATENT & TM OFFICE

PALM III APPLICATION FILE DATA CODING SHEET

041994

FORMAT NO. 2 Serial No. 09/ TYPE APPL 7 FILING DATE Month 04 Day 24 Year 98 SPECIAL HANDLING GROUP ART UNIT 2631 CLASS 375 SHEETS OF DRAWINGS 02 ASGT? N TOTAL CLAIMS 018 INDEPENDENT CLAIMS 003 SMALL ENTITY? Y FILING FEE RECEIVED 0170 SECURITY FOREIGN CASE? LICENSE? N

FORMAT NO. 3 ATTORNEY/DOCKET NUMBER (12 spaces) 5525-101 Appl.'s Reg. Nos. APPL. PAPERS CODING SHEET FORMAT NO. 4 Applicant's Name & Address APPL. PAPERS CODING SHEET FORMAT NO. 5 Title of Invention APPL. PAPERS CODING SHEET FORMAT NO. 6&7 Correspondence Address APPL. PAPERS CODING SHEET

FORMAT NO. 8

	CONTINUITY CODE	PARENT APPLICATION SERIAL NUMBER	STATUS CODE	PARENT FILING DATE Month Day Year	PARENT PATENT NUMBER
RECORD 801		0			
RECORD 802		0			
RECORD 803		0			
RECORD 804		0			
RECORD 805		0			
RECORD 806		0			
RECORD 807		0			
RECORD 808		0			
RECORD 809		0			
RECORD 810		0			

☐ MORE ON SUPPLEMENTAL CODING SHEET

FORMAT NO. 9

	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FILING DATE Month Day Year
RECORD 901			
RECORD 902			
RECORD 903			
RECORD 904			
RECORD 905			
RECORD 906			
RECORD 907			
RECORD 908			
RECORD 909			
RECORD 910			

FOREIGN PRIORITY CLAIMED? ☐ YES ☒ NO

☐ APPLICATION PAPERS

☐ MORE ON SUPPLEMENTAL CODING SHEET

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SEARCHED

Class	Sub.	Date	Exmr.
357	23.8 23.4 46	7/87	JJ
~~plate~~		8/88	JJ
357	22		

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
357	23.4 23.8 46 22	8/88	JJ

SEARCH NOTES

	Date	Exmr.

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INDEX OF CLAIMS

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SYMBOLS

= ..... Rejected

= ..... Allowed

(through numeral) Canceled

= ..... Restricted

= ..... Non-elected

= ..... Interference

= ..... Appeal

= ..... Objected

PATENT APPLICATION SERIAL NO. 041994

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

050 04/30/87 041994 1 201 170.00 CK

170.00 201 a

41994 PATENT

Case Docket No. SS-520-01

Date April 20, 1987

THE COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor: Klas H. Eklund

For: HIGH VOLTAGE MOS TRANSISTORS

Enclosed are:

11 Pages of specification 1 Pages of abstract 5 Pages of claims

2 Sheets of drawing ____ formal x informal

____ An assignment of the invention to _____

_____

____ A certified copy application(s) _____

_____ from which priority is claimed.

CLAIMS AS FILED				
	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE $340.00
Total Claims	18 -20 =	0	x $12.00	0
Independent Claims	3 -3 =	0	x $34.00	0
Multiple Dependent Claims, if any			$110.00	0

Filing Fee $ 340.00

[X] A verified statement that this is a filing by a small entity is attached.
The fee due is fifty percentum of the above.

Filing Fee $ 170.00

[X] The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

[X] A check in the amount of $170.00 ; ____ This includes $7.00 for recording the assignment.

Attorney for Applicant

Reg. No.: 22,611

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, CA 95054
(408) 727-7077

041,994

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

To the Commissioner of Patents and Trademarks:

Your petitioner, KLAS H. EKLUND, a citizen of Finland and resident of Los Gatos, California, whose post office address is 243 Mistletoe Road, 95030, prays that letters patent may be granted to him for

501

HIGH VOLTAGE MOS TRANSISTORS

set forth in the following specification.

041994

High Voltage MOS Transistors

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance,

the net number of charges should be around $1x10^{12}/cm^2$. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of $R_{on}xA$ (where R_{on} is the on-resistance in the linear region and A is the area taken up by the device). For an n-channel device in the voltage range of two hundred fifty to three hundred volts, $R_{on}xA$ is typically 10 - 15 $\Omega\,mm^2$. A discrete vertical D-MOS device in the same voltage range has a figure of merit of 3 $\Omega\,mm^2$, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage devices.

SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit, R_{on} x A, of about 2.0 $\Omega\,mm^2$,

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (JFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an n-channel device, voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about 2.0 Ω mm^2.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

IN THE DRAWINGS

Fig. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present invention.

Fig. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present invention.

Fig. 3 is a diagrammatic view of the transistors shown in Figs. 1 and 2 forming a complementary pair on the same chip.

Fig. 4 is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in Fig. 3.

Fig. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at Fig. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p^+ material and a pocket 21 of n^+ material are diffused into the p^- substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact 16, a pocket 24 of n^+ material is diffused into the substrate. An

extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p- material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from $1 \times 10^{12}/cm^2$ to around $2 \times 10^{12}/cm^2$, or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch off

voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two - four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of $5 \times 10^{16} - 1 \times 10^{17}/cm^3$. At doping levels above $10^{16}/cm^3$, the mobility starts to degrade. and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around $1 \times 10^{12}/cm^2$ and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of merit, $R_{on} \times A$, of about $2.0\ \Omega mm^2$ for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about $10 - 15\ \Omega mm^2$, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of $3 - 4\ \Omega mm^2$.

With reference to Fig. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 32 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n^+ type material and a pocket 36 of p^+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from beneath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p^+ drain contact pocket 38 and the n-well.

Looking now at Fig. 3, an n-channel transistor 10, similar to that shown in Fig. 1, and a p-channel transistor 30, similar to that shown in Fig. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to Figs. 1 and 2, no further description is considered necessary.

As shown in Fig. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in Fig. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p^+ pocket 49 and an n^+ pocket 51 are provided in the p^- substrate beneath the source contact. The n^+ pocket extends to beneath the gate. An n^+ pocket 52 is provided

beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n^+ pocket 58 and a p^+ pocket 59 are provided in the n-well beneath the source contact and a p^+ pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

Fig. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysilicon gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71 is provided beneath the source contact and an n^+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dixode layer thereabove. Beneath the drain contact is an n^+ type pocket 74 and an n-type extended drain region 76. A top layer ~~72~~ 73 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the

punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source an an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an n-channel device, and has a figure of merit, $R_{on} \times A$, of about 2.0 Ωmm^2. The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all

alterations and modifications as fall within the true spirit and scope of the invention.

12 Cm I claim:

IN THE CLAIMS

1. A high-voltage MOS transistor comprising an insulated-gate field-effect transistor, and a double-sided junction-gate field-effect transistor connected in series, said transistors being united in one structure.

2. In a high-voltage MOS transistor having a source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the insulated-gate device and the drain, said extended drain region being formed on material having a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, said top layer of material and said material beneath the extended drain region being interconnected with the source for applying a reverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conductivity-type materials.

3. A high-voltage MOS transistor comprising a source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the insulated gate device and the drain, said extended drain region being formed on material having a

conductivity-type opposite that of the extended drain region, and a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, said top layer of material and said material beneath the extended drain region being interconnected with the source for applying a reverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conductivity-type materials.

4. The high-voltage MOS transistor of claim 1 further including,

another high-voltage MOS transistor of opposite conductivity-type forming a complementary pair on the same chip.

5. The high-voltage MOS transistor of claim 2 wherein,

said layer on top of the extended drain region is an ion-implantation.

a 6. The high-voltage MOS transistor of claim 4 wherein,

said top layer has a depth of one-micron or less.

a 7. The high-voltage MOS transistor of claim 4 wherein,

said top layer has a doping density higher than 5 x $10^{16}/cm^3$ so that the mobility starts to degrade.

8. The high-voltage MOS transistor of claim 3 wherein,

said extended drain is made of n-type conductive material and said top layer is made of p-type conductive material.

9. The high-voltage MOS transistor of claim 3 wherein,

said extended drain is made of p-type conductive material and said top layer is made of n-type conductive material.

10. The high-voltage MOS transistor of claim 9 wherein,

said transistor is embedded in a well of n-type conductive material in a substrate of p-type conductive material, and further including a complementary high-voltage MOS transistor having an extended drain of n-type conductive material embedded in the substrate.

11. The high-voltage MOS transistor of claim 3 wherein,

both the extended drain region and the top layer of material are diffusions or ion implantations into a substrate or epitaxial layer.

12. The high-voltage MOS transistor of claim 11 wherein,

said extended drain region and the top layer of material are formed by using the same mask (self alignment).

13. The high-voltage MOS transistor of claim 3 wherein,

the material on which the extended drain region is formed is a substrate; and

the substrate is of one conductivity-type material, and further including a complementary transistor embedded in a well or epi-island of opposite conductivity-type material on the same substrate.

14. The complementary pair of high-voltage MOS transistors of claim 13 wherein,

the well in which the complementary transistor is embedded is the same diffusion as the extended drain for the other transistor.

15. The complementary pair of high-voltage MOS transistors of claim 14 wherein,

the well is an n-well and further used for a low voltage p-channel device.

16. The high-voltage MOS transistor of claim 2 wherein,

the top layer is floating.

17. The high-voltage MOS transistor of claim 3 wherein,

the source region and the drain region are formed in a similar manner.

18. The high-voltage MOS transistor of claim 3 further including,

low voltage logic and analog function on the same chip.

add q2

ABSTRACT OF THE DISCLOSURE

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HIGH VOLTAGE MOS TRANSISTORS

the specification of which

[X] is attached hereto.

[ ] was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Thomas E. Schatzel Reg. No. 22,611
Douglas R. Millett Reg. No. 31,784

Address all telephone calls to Thomas E. Schatzel at telephone No. (408) 727-7077.

Address all correspondence to:

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
10211 Scott Boulevard, Suite 201
Santa Clara, California 95054-3093

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter to each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: 401-SP KLAS H. EKLUND

Inventor's Signature: _____ Date: 4/7/87

Residence: 243 Mistletoe Road Los Gatos, California 95030

Citizenship: Finland

Post Office Address: 243 Mistletoe Road Los Gatos, California 95030

041994

Applicant or Patentee: KLAS H. EKLUND
Serial or Patent No.:
Filed or Issued:
Attorney's Docket No.: 520-01
For: HIGH VOLTAGE MOS TRANSISTORS

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c) - INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled HIGH VOLTAGE MOS TRANSISTORS described in

[X] the specification filed herewith
[ ] application serial no. _____, filed _____
[ ] patent no. _____, issued _____.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

[X] no such person, concern, or organization
[ ] persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

FULL NAME n/a
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME n/a
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME n/a
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
KLAS H. EKLUND		
Signature of Inventor	Signature of Inventor	Signature of Inventor
4/17/87		
Date	Date	Date

041994

KLAS H. EKLUND

55-520-01

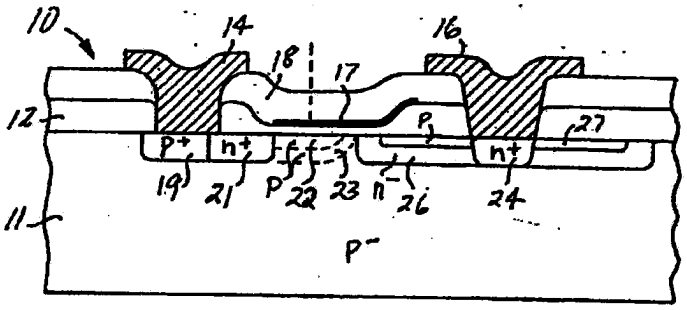

Fig. 1

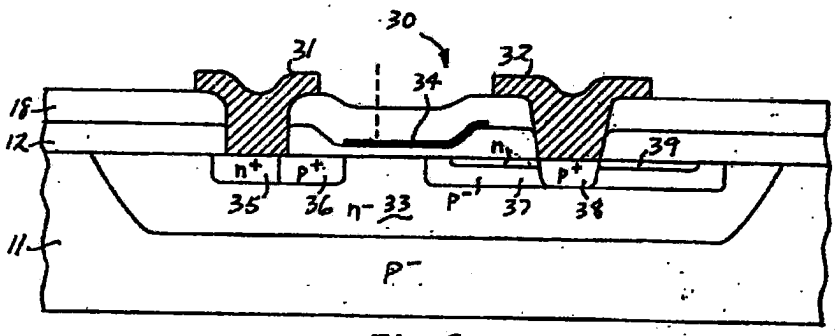

Fig. 2

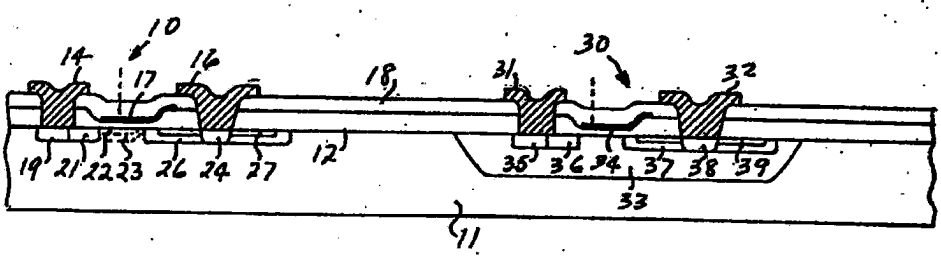

Fig. 3

(5 Fig)

041994

KLAS H. EKLUND

SS-520-01

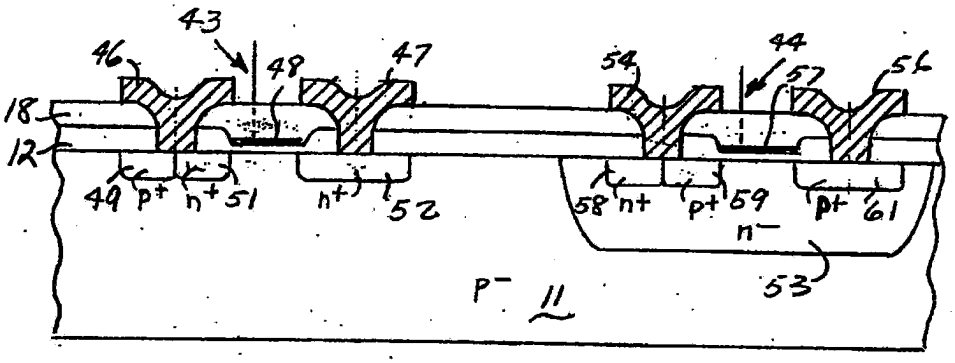

Fig_4

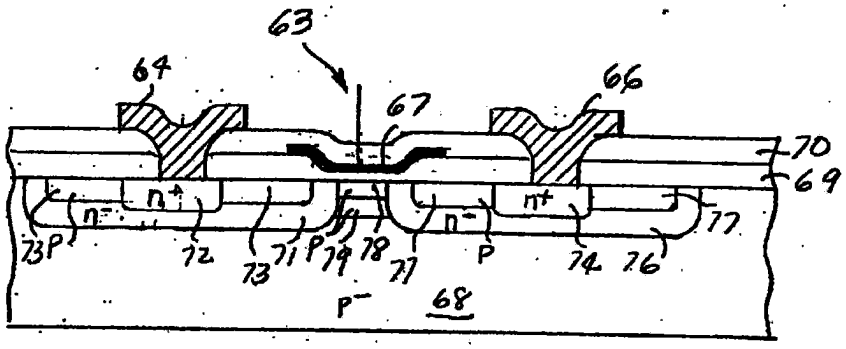

Fig_5

357/43
Jackson
KLAS H. EKLUND

Print Of Drawing
As Original Filed

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Conventional NLDS

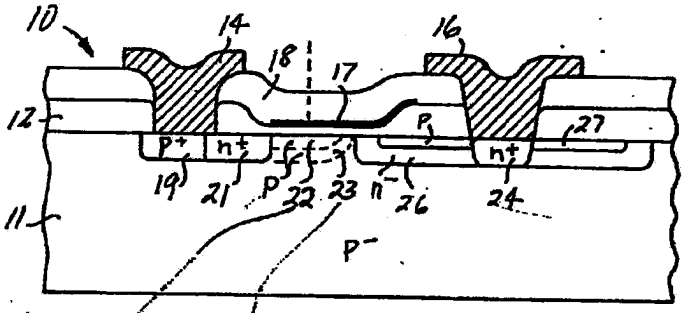

Fig-1

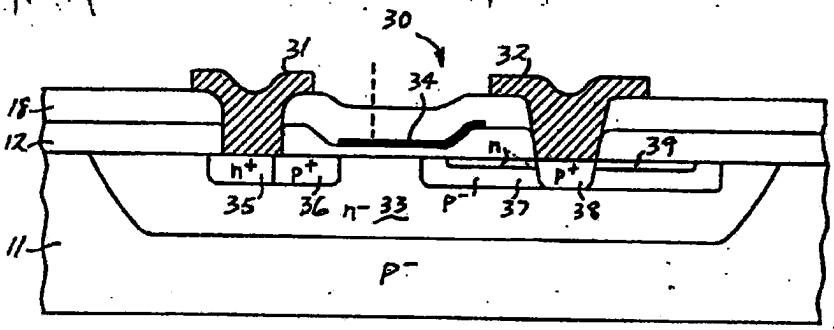

Fig-2

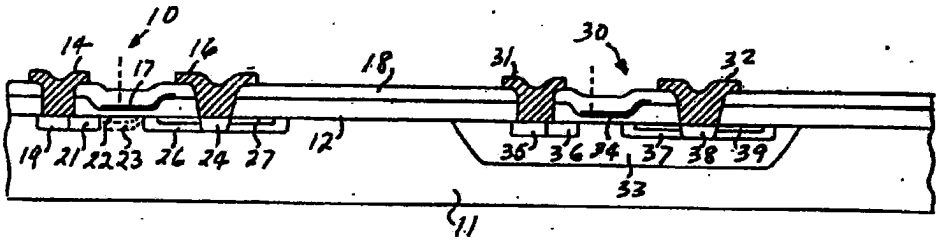

Fig 3

Print Of Drawing
As Original Filed

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2 OF 2
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KLAS H. EKLUND

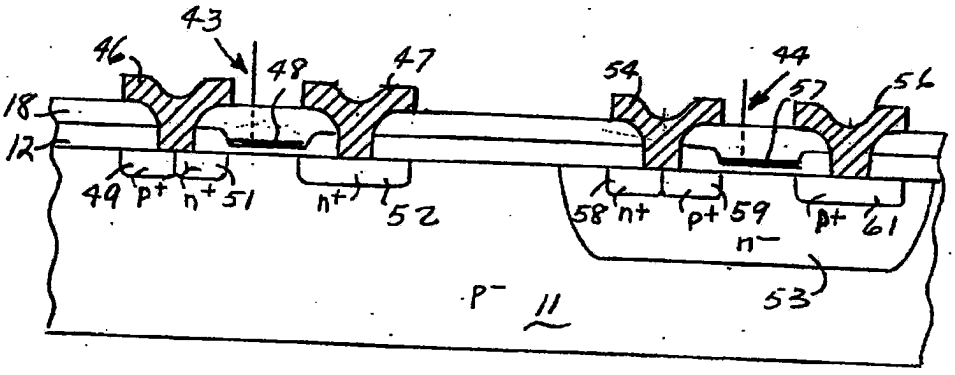

Fig-4

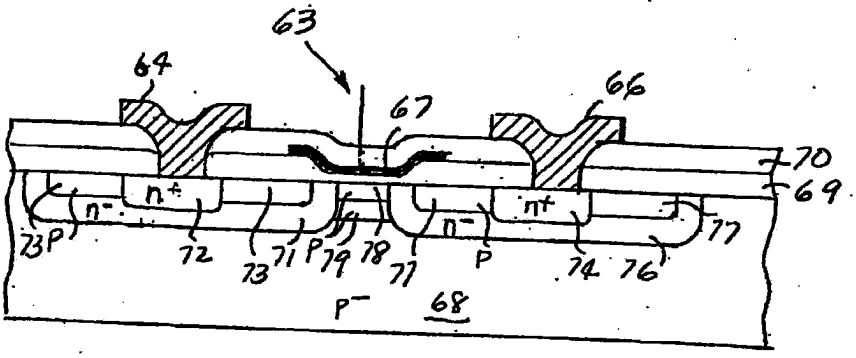

Fig-5

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	ERLUND K	86-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON DAVID	
ART UNIT	PAPER NUMBER
233	2

DATE MAILED: 12/07/87

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-18 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-18 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

On page 9 line 28 "72" should be --73--.

Claims 1, 2, 4-7, 16 are rejected under 35 U.S.C. 112, first and second paragraphs, as the claimed invention is not described in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same, and/or for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The structure of claim 1 is indefinite. The language "being united in one structure" is vague and indefinite and does not clearly or concretely define the structure of applicant's invention. The terms "insulated gate FET" and "double sided JFET" are also broad and do not define applicant's invention. Claim 2 is confusing since lines 14-17 mimic lines 17-20. The other claims are rejected for dependence on 1 or 2.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP 608.01(o). Correction of the following is required: there is no proper antecedent in the specification for the process descriptions of claims 11, 13, 14, 17.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless-
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international

application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-3, 5-9, 11, 12, 16 rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Colak shows a DMOS device wherein layer 16 may perform the function of a JFET gate "on top of" an extended drain region 14 in the embodiment of figs. 2B or 2C. Substrate layer 12 may act as the other gate of the JFET. Clearly claim 1 does not distinguish over Colak. Note that mere labels as "JFET" do not structurally distinguish the claims over Colak since the structure of Colak may be labeled an IGFET in series with a double sided JFET as shown above. Claim 2 also does not distinguish over Colak since the claimed structure is shown in Colak and the intended use language "whereby current flow..." in claim 2 does not structurally distinguish over Colak and furthermore Colak's device may perform the same intended function. See In re Pearson 181 USPQ 642 or Ex parte Minks 169 USPQ 120 on statements of intended use in claims drawn to structure as we have here. Similarly claim 3 does not distinguish over Colak. Claim 5 is a product by process claim which does not structurally distinguish applicant's final product over Colak.

A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re. Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re

Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by Process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim 6 also is undistinguishing over Colak since the thickness of layer 16 is a design variable and 1 micron thickness would not be unobvious to one of ordinary skill in view of Colak. Similarly, in re claim 7 a dopant density of greater than $5x10^{16}$/cc would not be unobvious for the doping density of layer 16 of Colak. Claims 8, 9 also are obvious over Colak. Claims 11, 12 are product by process claims which also do not distinguish the final product over Colak. Claim 16 also does not distinguish over Colak as "floating" is vague and undistinguishing.

The following is a quotation of 35 U.S.C. "103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at

the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 4, 10, 13-15, 17 and 18 rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

Thomas shows the obvious of providing low voltage and high voltage devices on the same substrate. It would be obvious from Thomas to practice Colak as CMOS or with other devices. Claim 4 is hence obvious. In re claims 10, 13, 15 "well" regions are also obvious from Thomas. Claims 14, 17 also are product by process claims which do not distinguish the final product over the suggestions of the references on final structure. Claim 18 also does not distinguish over the suggestions of Colak in view of Thomas.

Any inquiry concerning this communication should be directed to J. Jackson at telephone number 703-557-4824.

Jackson/EW
12-2-87

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253

PTO - 948
(Rev. 9-92)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTACHMENT TO PAPER NUMBER 2

GROUP 260

S.N. 41994

NOTICE OF PATENT DRAWINGS OBJECTION

Drawing Corrections and/or new drawings may only be submitted in the manner set forth in the attached letter, "Information on How to Effect Drawing Changes" PTO-1474.

A. ☒ The drawings, filed on 1/24/97, are objected to as informal for reason(s) checked below:

1. ☐ Lines Pale.
2. ☐ Paper Poor.
3. ☒ Numerals Poor.
4. ☒ Lines Rough and Blurred. FIG 1-5
5. ☐ Shade Lines Required.
6. ☐ Figures Must be Numbered.
7. ☐ Heading Space Required.
8. ☐ Figures Must Not be Connected.
9. ☐ Criss-Cross Hatching Objectionable.
10. ☐ Double-Line Hatching Objectionable.
11. ☐ Parts in Section Must Be Hatched.
12. ☐ Solid Black Objectionable.
13. ☐ Figure Legends Placed Incorrectly.
14. ☐ Mounted Photographs.
15. ☒ Extraneous Matter Objectionable. [37 CFR 1.84 (l)] BORDER LINES
16. ☐ Paper Undersized; either 8½" x 14", or 21.0 cm. x 29.7 cm. required.
17. ☐ Proper A4 Margins Required:
    ☐ TOP 2.5 cm. ☐ RIGHT 1.5 cm.
    ☐ LEFT 2.5 cm. ☐ BOTTOM 1.0 cm.
18. ☐ Other:

B. ☒ The drawings, submitted on 4/24/98, are so informal they cannot be corrected. New drawings are required. Submission of the new drawings MUST be made in accordance with the attached letter.

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP--APART AND DISCARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
041,994	253	2

APPLICANT(S): Ekl/und

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4,626,879	12/86	Colak	357	23.8	12/82
	B	4,628,341	12/86	Thomas	357	23.8	9/85
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE
J. Jackson	11/87

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

3

#75.00-216-#3253

PATENT

Case Docket No. SS-1520-01

Date April 7, 1988

In re application of: Klas H. Eklund

Serial No.: 07/041,994

Filed: April 24, 1987

For: HIGH VOLTAGE MOS TRANSISTORS

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

[ ] No additional fee is required. [X] Two Month Extension Fee Enclosed. ($85.00)

[ ] Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Addtnl. Fee
Total Claims	_____	Minus	_____ =	____ x	$12.00	= _____
Indep. Claims	_____	Minus	_____ =	____ x	$34.00	= _____

Additional Fee Due $ _____

[X] A verified statement claiming small entity status "X" has been filed; _____ is attached. The fee due is fifty percentum of the above.

Fee Due $ _____

[X] A check in the amount of $ 85.00 is attached. (Two Month Extension Fee)

[X] Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

040 04/13/88 041994
Attorney For Applicant

By [redacted]
Reg. No.: 22,611

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard Suite 201
Santa Clara, CA 95054
(408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88 (Date of Deposit)

Thomas E. Schatzel
Name of Applicant, Assignee or Registered Rep.

[signature] 4/7/88
Signature Date

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Serial No.: 07/041,994

Filed : 04-24-87

For : HIGH VOLTAGE MOS TRANSISTORS

Group Art Unit: 253

Examiner: J. Jackson

Attorneys Docket No.: SS-520-01

COMMISSIONER OF PATENTS & TRADEMARKS
Washington, D.C. 20231

Date of this Paper:
April 7, 1988

AMENDMENT

In response to the U.S. Patent Office Action mailed December 7, 1987 (Paper No. 2), please amend this application as follows:

In the Specification

Page 1, line 26, change "of" to --on--;

Page 9, line 15, insert the following paragraph:

--It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one complimentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.--.

A1

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88
(Date of Deposit)
Thomas E. Schatzel
Name of Applicant, assignee, or Registered Rep.
Signature 4/7/88 Date

Page 9, line 28, change "72" to --73--.

In the Claims

Cancel claims 1-5 and 8-18.

Add new claims 19-23 as follows:

19. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact connected to one pocket,

a drain contact connected to the other pocket,

an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

20. The high voltage MOS transistor of claim 19 having one channel conductivity type in combination with a ~~complimentary~~ complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

21. The high voltage MOS transistor of claim 19 combined on the same chip with a low voltage CMOS implemented device.

22. The combination of claim 21 further including,

a ~~complimentary~~ complementary high voltage MOS transistor, and

a ~~complimentary~~ complementary low voltage CMOS implemented device on the same chip and isolated from each other.

23. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact connected to one pocket,

an extended source region of the second conductivity type extending laterally each way from the source contact pocket to surface-adjoining ~~position~~ positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,

said top layer and said substrate being subject to application of a reverse-bias voltage,

a drain contact connected to the other pocket,

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an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,

a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

Amend the claims as follows:

Claim 6, line 1, change "5" to --19--; and

Claim 7, line 1, change "5" to --19--.

REMARKS

The specification has been amended to correct minor errors and to provide an antecedent basis in the specification for epitaxial layer and epi-island mentioned in former claims 11 and 13.

This invention relates to high voltage, metal oxide semiconductor transistors of the field effect type. There is a need for more efficient transistors which can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The

integrated devices should be easily combined with low voltage (five volt) control logic on the same chip. Devices of opposite conductivity should be combinable in a complimentary manner on the same chip. Such transistors, with modifications, should be capable of source-follower applications.

The applicant has disclosed a novel and unobvious high voltage MOS transistor having a low threshold voltage that is compatible with five volt control logic and a low ON-resistance. This transistor can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The high voltage MOS transistors can be modified for source-follower applications by providing both extended source regions and extended drain regions. These transistors are formed on a substrate of a first conductivity type having a surface. A pair of laterally spaced pockets of semiconductor material of a second conductivity type are provided within the substrate and adjoining the substrate surface. A source contact is connected to one pocket and a drain contact is connected to the other pocket. An extended drain region of a second conductivity type extends laterally each way from the drain pocket to surface-adjoining positions. A layer of material of the first conductivity type is provided on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The top layer of material and the substrate are subject to application of a reverse-bias voltage. None of the cited references show such structure.

Colak, U.S. Patent No. 4,626,879, shows a DMOS transistor suitable for source follower applications. This device has a substrate with three epitaxial layers formed thereon. A surface-adjoining channel region is diffused into the epitaxial layers and a source region is diffused into the channel diffusion above the channel region. A drain region is diffused into the top epitaxial layer. An extended drain

region is formed from a portion of the top epitaxial layer between the drain region and the channel region. The top and bottom epitaxial layers are interconnected, and the bottom layer may operate as a parallel extended drain region between the connection points. The intermediate epitaxial layer may operate as an extended drain region in a dual-gate/dual-drain structure wherein all three epitaxial layers contribute to device conductivity for achieving optimum normalized "ON" resistance.

Thomas, U.S. Patent No. 4,628,341 shows an integrated circuit structure that includes both low-voltage n-channel and p-channel MOS transistors and high voltage n-channel and p-channel MOS transistors.

The claims are now clearly distinguished from the cited references. New claim 19 recites "an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions, a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions". When high voltage n-channel and p-channel devices are combined on the same chip with low voltage control logic, this structure isolates the devices from each other. Claim 19 also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional MOS transistors and is thus, distinguished from DMOS devices which require a higher threshold voltage. The structure of claim 19 enables a lower threshold voltage, compatibility with five volt control logic, and eliminates the need for an additional power supply and interface circuit.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and thus, can be distinguished for the same reasons as claim 19.

Claim 23 is directed to the transistor, shown in Fig. 5 of the drawings, that has been modified for source-follower applications by providing both extended source and drain regions. Top layers cover intermediate portions of the extended source and drain regions. The top layers and substrate are subject to application of a reverse-bias voltage.

Accordingly, claims 6-7 and 20-23 are patentably distinct from the cited references and allowance of these claims is requested.

If the Examiner is of the opinion that a telephone conference with applicant's attorney would expedite matters, such a conference is invited.

Respectfully submitted,

Reg. No. 22,611

By _____
Thomas E. Schatzel

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054
Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88
(Date of Deposit)

Thomas E. Schatzel
Name of applicant, assignee, or Registered Rep.

_____ 4/7/88
Signature Date

Serial No.: 07/041,994
Filed: 4-24-87
Attnys. Docket No.: SS-520-01

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

___ other than a small entity

____ verified statement attached

__X__ small entity

__X__ verified statement already filed

Payment of fees

__X__ The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please ____also __X__ do not charge issues fees under 37 C.F.R. 1.18 to Account No. 19-0310.

Reg. No. 22,611

Attorney for Applicant

Telephone: (408) 727-7077

Law Offices of Thomas E. Schatzel
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

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Thomas E. Schatzel
Name of applicant, assignee, or Registered Representative

Signature 4/7/88 Date

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	EKLUND K	SS-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
253	4

DATE MAILED: 06/17/88

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 4/11/88 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 6,7, 19-23 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 6,7, 19-23 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received
    ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7 - 82) EXAMINER'S ACTION

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless-
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 19, 6, 7 are rejected under 35 U.S.C. 102 (e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Claim 19 still does not distinguish over Colak. See figures 1, 2B and 2C of Colak where 22 and 24 define "pockets", layers 18 and 14 form an "extended drain" which extends to the surface "each way" from the drain contact 24, layer 16 defines a layer of material of first conductivity type "on top of" extended drain layer 14, and layer 16 and substrate 12 are subject to application of a reverse bias voltage during operation of the device. Note that layer 16 is connected to the source and the substrate is reverse biased through SS. Thus claim 19 does not distinguish over Colak. Claim 5 is undistinguishing since Colak teaches a layer 16 thickness of 2 micron for 400 V operation, however, for lower voltage operation design layer 16 would be thinner, and 1 micron thickness is thus an obvious design variant to the artist. Similarly, to the artist, the design of claim 7 is obvious in view of Colak who teaches $10^{16}/cm^3$ for layer 16.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 20-23 are rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

As stated in the previous rejection, Thomas shows that high voltage fet devices (as Colak) are advantageously formed complementary and also integrated with low voltage devices. Hence claims 20-22 are obvious.

Claim 23 is rejected under 35 U.S.C. 103 as being unpatentable over Sze.

Colak teaches punch through and avalanche protection layer 16 for a DMOS device. To one of ordinary skill it would have been obvious to practice the teachings of Colak in other MOS devices as ordinary fets as shown in Sze. Note figures 3, 51 or 52 of Sze where the source or drain are structurally similar and their function is dependent on the particular voltage applied. Hence, to the artist it would be obvious to apply the

teachings of Colak to symmetrical ordinary fets as shown in Sze to provide higher voltage operation.

Applicant's arguments filed April 11, 1988 have been fully considered but they are not deemed to be persuasive.

Applicant's argument that Colak does not show a drain "extending laterally each way" from the drain is not convincing as shown in the above rejection.

Clearly there is drain material 18 on each side of pocket 24.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, THIS ACTION IS MADE FINAL. See MPEP 706.07(a).

Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Jackson whose telephone number is (703) 557-4824.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 557-3311.

J. Jackson:klw

6-15-88

(703) 557-4824

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253

TO SEPARATE, H[illegible]D TOP AND BOTTOM EDGES, SNAP-APART AND R[illegible]CARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
041994	253	4

APPLICANT(S): Eklund

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	Sze, Physics of Semiconductor Devices Wiley & Sons N.Y. ©1981 pp 431-438, 486-491 (14) (14)
S	
T	
U	

EXAMINER	DATE
J. Jackson	6/88

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	EKLUND K	SS-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
259	5

DATE MAILED: 08/11/88

EXAMINER INTERVIEW SUMMARY RECORD

All participants (applicant, applicant's representative, PTO personnel):

(1) Jack Edwards (3) Klas H. Eklund

(2) Thomas E. Schatzel (4) Jerome Jackson

Date of interview 10 August 1988

Type: ☒ Telephonic ☐ Personal (copy is given to ☐ applicant ☐ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No. If yes, brief description: _____

Agreement ☒ was reached with respect to some or all of the claims in question. ☐ was not reached.

Claims discussed: all

Identification of prior art discussed: Colak

Description of the general nature of what was agreed to if an agreement was reached, or any other comments: New amendments to the claims to be submitted distinguishing applicant's channel structure and surface adjoining layer 27 over Colak.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.).

Unless the paragraphs below have been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW (e.g., items 1—7 on the reverse side of this form). If a response to the last Office action has already been filed, then applicant is given one month from this interview date to provide a statement of the substance of the interview.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview.

☐ Since the examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action.

Jerome Jackson Jr.
Examiner's Signature

PTOL-413 (rev. 1-81)

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#6

PATENT

HAND CARRIED TO PTO

Case Docket No. SS-520-01

Date August 12, 1988

In re application of: Klas H. Eklund

Serial No.: 07/041,994

Filed: April 24, 1987

For: HIGH VOLTAGE MOS TRANSISTORS

ATTN: BOX A.F.
COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment After Final for the above application.

[X] No additional fee is required.

[ ] Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Addtnl. Fee
Total Claims	_____	Minus	_____ =	_____ x	$12.00	= _____
Indep. Claims	_____	Minus	_____ =	_____ x	$34.00	= _____

Additional Fee Due $ _____

[X] A verified statement claiming small entity status x has been filed; _____ is attached. The fee due is fifty percentum of the above.

Fee Due $ _____

[ ] A check in the amount of $_____ is attached.

[X] Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

By _____
Reg. No.: 22,611

Attorney For Applicant

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard Suite 201
Santa Clara, CA 95054
(408) 727-7077

88 6/15
8/88

PATENT 8-15-88

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund
Serial No.: 07/041,994
Filed: : April 24, 1987
For : HIGH VOLTAGE MOS TRANSISTORS

Group Art Unit: 253
Examiner: J. Jackson, Jr.
Attorneys Docket No.: SS-520-01

ATTENTION: BOX A.F.

COMMISSIONER OF PATENTS
& TRADEMARKS
Washington, D.C. 20231

Date of this Paper:
August 12, 1988

AMENDMENT AFTER FINAL

In response to the U.S. Patent Office Action mailed June 17, 1988 (Paper No. 4), please amend this application as follows:

In the Claims

Claim 19, line 12, before "layer" insert --surface adjoining--;
line 22, before "region" insert --substrate--.
Claim 20, line 2, change "complimentary" to --complementary--.
Claim 22, line 2, change "complimentary" to --complementary--;
line 3, change "complimentary" to --complementary--.
Claim 23, line 9, delete "a";
line 10, change "position" to --positions--;
line 11, before "layer" insert --surface adjoining--;
line 18, delete "a";
line 20, before "layer" insert --surface adjoining--;
line 30, before "region" insert --substrate--.

REMARKS

The applicant appreciates the telephone interview on August 10, 1988, courteously granted by the Examiner.

Claim 19, as amended, now provides for an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions and a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The layer 16 of Colak is not surface-adjoining but is buried under layer 18. There is no layer of material of the first conductivity type on top of layer 18. Colak's layer 16 extends from beneath the drain contact pocket 24 to the channel region 20, and thus, is not between the drain contact pocket and the surface adjoining positions of the extended drain region.

Claim 19 also provides for the top layer of material and the substrate being subject to application of a reverse-bias voltage. Thus, the top layer and the substrate act as gates for controlling current flow through the extended drain region between the surface adjoining positions and the drain contact pocket. This structure can be considered a double-sided, junction-gate field-effect transistor (JFET). Colak shows a layer 14 intermediate a layer 16 and a substrate 12 that are subject to application of a reverse-bias voltage. Though this structure of Colak could be considered a double-sided JFET, layer 16 is not surface-adjoining as defined in claim 19. Colak's double-sided JFET is buried under layer 18 which is connected in parallel with layer 14 by semiconductor zones 16c, 16d. Layer 16 also acts as a gate for layer 18 so that layers 16 and 18 could be considered a single-sided JFET. Thus, the extended drain of Colak includes the single-sided JFET connected in parallel with the double-

sided JFET thereunder. Both the extended drain structure of claim 19 and Colak's drain structure have relatively high voltage capability. However, it is desirable to control the high voltage with relatively low voltage.

Claim 19 further provides for a substrate having a surface, an insulating layer on the surface of the substrate covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and a gate electrode on the insulating layer electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Thus, claim 19 is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device. The MOSFET structure has a lower threshold voltage than a D-MOS device (0.7 volts compared to two - four volts for the D-MOS device) and thus, is directly compatible with five volt logic. D-MOS devices usually require an additional power supply of ten to fifteen volts for driving the gate. The MOSFET structure has less on-resistance and thus, further reduces the total on-resistance of the combined structure (MOSFET plus double-sided JFET).

Claim 19 is directed to the structural combination of a double-sided JFET and a MOSFET so that a high voltage transistor can be controlled with relatively low voltage. Thus, claim 19 is patentably distinct over Colak.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and are thus patentably distinct from Colak for the same reasons as claim 19. While Thomas shows that high voltage FET devices are advantageously formed complementary and also integrated with low voltage devices, claims 20-22 are limited to transistors having the structure as defined in claim 19. This structure facilitates isolation of complementary high voltage devices and low voltage, C-MOS

implemented devices on the same chip. Isolation of the epitaxial layers shown by Colak from corresponding layers of a complementary device would be difficult.

Claims 6 and 7 include further limitations on the depth of the top layer and the doping density thereof. The depth is one-half or less than that disclosed by Colak for layer 16 and the doping density is at least five times greater. Furthermore, Colak's layer 16 is not similarly situated as the top layer of claim 19, and thus, is not comparable. Thus, claims 6 and 7 are patentably distinct from Colak for the same reasons as claim 19 and for the further limitations therein.

Claim 23 is directed to the transistor 63, shown in Fig. 5, that is suitable for source follower applications. This claim contains limitations similar to claim 19 for the MOSFET structure and the double-sided JFET about the drain contact pocket. It further includes structural limitations for a double-sided JFET about the source contact pocket. While the book by Sze discloses MOSFET structures having sources and drains that are similar to each other, such sources and drains are not similar to the double-sided JFET structures disclosed by the applicant and specifically claimed structurally in claim 23. Thus, claim 23 is patentably distinguished from Sze.

Should the Examiner be of the opinion that a telephone conference with applicant's attorney would be beneficial, he is invited to contact the undersigned at the number set out below.

Respectfully submitted,

Reg. No. 22,611 By _____
Thomas E. Schatzel

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054
Telephone: (408) 727-7077

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

___ other than a small entity

____ verified statement attached

_x_ small entity

_x_ verified statement already filed

Payment of fees

_X_ The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please ____also charge issues fees under 37 C.F.R. 1.18 _X_ do not to Account No. 19-0310.

Reg. No. 22,611

Attorney for Applicant

Telephone: (408) 727-7077

Law Offices of Thomas E. Schatzel
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

7

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	EKLUND K	SB-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
253	7

DATE MAILED: 8-25-88 ~~08/16/88~~

NOTICE OF ALLOWABILITY

PART I.
1. [X] This communication is responsive to Amend B 7/15/88
2. [X] All the claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
3. [X] The allowed claims are 6, 7, 19-23
4. [ ] The drawings filed on _____ are acceptable.
5. [ ] Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has [_] been received. [_] not been received. [_] been filed in parent application Serial No. _____, filed on _____
6. [ ] Note the attached Examiner's Amendment.
7. [ ] Note the attached Examiner Interview Summary Record, PTOL-413.
8. [ ] Note the attached Examiner's Statement of Reasons for Allowance.
9. [ ] Note the attached NOTICE OF REFERENCES CITED, PTO-892.
10. [ ] Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II.
A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

1. [ ] Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
2. [X] APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
   a. [X] Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No. 2 CORRECTION IS REQUIRED.
   b. [ ] The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED.
   c. [ ] Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
   d. [ ] Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:
- Examiner's Amendment
- Examiner Interview Summary Record, PTOL-413
- Reasons for Allowance
- Notice of References Cited, PTO-892
- Information Disclosure Citation, PTO-1449
- Notice of Informal Application, PTO-152
- Notice re Patent Drawings, PTO-948
- Listing of Bonded Draftsmen
- Other

JJ

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 2

PTOL-37 (REV. 2-88)

USCOMM-DC 85-3744

XL-85 (REV 4-88)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

All communications regarding this application should give the serial number, date of filing, name of applicant, and batch number.

Please direct all communications to the Attention of "OFFICE OF PUBLICATIONS" unless advised to the contrary.

The application identified below has been examined and found allowable for issuance of Letters Patent. PROSECUTION ON THE MERITS IS CLOSED.

	SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
	07/041,994	04/24/87	007	JACKSON JR, J	253	08/25/88
First Named Applicant	EKLUND,		KLAB H.			

TITLE OF INVENTION: HIGH VOLTAGE MOS TRANSISTORS

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
	SB-520-01	357-046.000	L66	UTILITY	YES	$280.00	11/25/88

The amount of the issue fee is specified in 37 C.F.R. 1.18. If the applicant qualified for and has filed a verified statement of small entity status in accordance with 37 C.F.R. 1.27, the issue fee is one-half the amount for non-small entities. The issue fee due printed above reflects applicant's status as of the time of mailing this notice. A verified statement of small entity status may be filed prior to or with payment of the issue fee. However, in accordance with 37 C.F.R. 1.28, failure to establish status as a small entity prior to or with payment of the issue fee precludes payment of the issue fee in the amount so established for small entities and precludes a refund of any portion thereof paid prior to establishing status as a small entity.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE as indicated above. The application shall otherwise be regarded as ABANDONED. The issue fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office. Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of the notice of allowance, the issue fee is charged to the deposit account at the time of mailing of this notice in accordance with 37 C.F.R. 1.311. If the issue fee has been so charged, it is indicated above.

In order to minimize delays in the issuance of a patent based on this application, this Notice may have been mailed prior to completion of final processing. The nature and/or extent of the remaining revision or processing requirements may cause slight delays of the patent. In addition, if prosecution is to be reopened, this Notice of Allowance will be vacated and the appropriate Office action will follow in due course. If the issue fee has already been paid and prosecution is reopened, the applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a deposit account.

In the case of each patent issuing without an assignment, the complete post office address of the inventor(s) will be printed in the patent heading and in the Official Gazette. If the inventor's address is now different from the address which appears in the application, please fill in the information in the spaces provided on PTOL-85b enclosed. If there are address changes for more than two inventors, enter the additional addresses on the reverse side of the PTOL-85b.

The appropriate spaces in the ASSIGNMENT DATA section of PTOL-85b must be completed in all cases. If it is desired to have the patent issue to an assignee, an assignment must have been previously submitted to the Patent and Trademark Office or must be submitted not later than the date of payment of the issue fee as required by 37 C.F.R. 1.334. Where there is an assignment, the assignee's name and address must be provided on the PTOL-85b to ensure its inclusion in the printed patent.

Advance orders for 10 or more printed copies of the prospective patent can be made by completing the information in Section 4 of PTOL-85b and submitting payment therewith. If use of a deposit account is being authorized for payment, PTOL-85c should also be forwarded. The order must be for at least 10 copies and must accompany the issue fee. The copies ordered will be sent only to the address specified in section 1 or 1A of PTOL-85b.

☒ Note attached communication from the Examiner.

☐ This notice is issued in view of applicant's communication filed _____

IMPORTANT REMINDER

Patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. See 37 CFR 1.20 (e)—(g).

PATENT AND TRADEMARK OFFICE COPY

8

Patent
11-10-88

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eklund, Klas H.
Filed : 04/24/87
Examiner : Jackson Jr.,
Group Art Unit : 253
Atty Docket No.: SS-520-01
For : "HIGH VOLTAGE MOS TRANSISTORS"

Issue Batch No.: L66
Allowance Date 08/25/88
Serial No. : 07/041,994

Box Issue Fees
COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D. C. 20231

Date of This Paper
October 19, 1988

FORMAL DRAWING TRANSMITTAL

Transmitted herewith are formal drawings for the above identified application as requested in the Notice of Allowance, Paper No. 7, mailed August 25, 1988. Corrections have been made as requested by the Examiner. Applicant respectfully requests that the formal drawings be filed.

Respectfully submitted,

By: Thomas E. Schatzel
Reg. No. 22,614

Attorney for Applicant

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, CA 95054-3093

Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 10/19/88 (Date of Deposit)
Thomas E. Schatzel
Name of applicant, assignee, or Registered Representative
Signature 10/19/88 Date

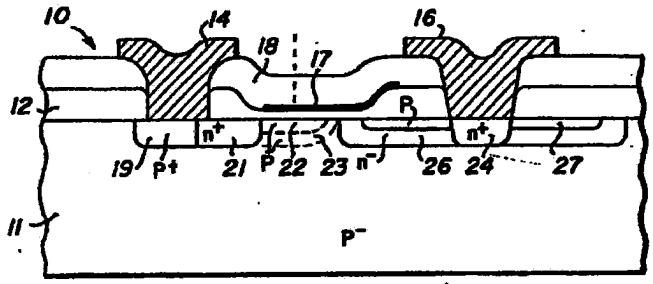

Fig_1

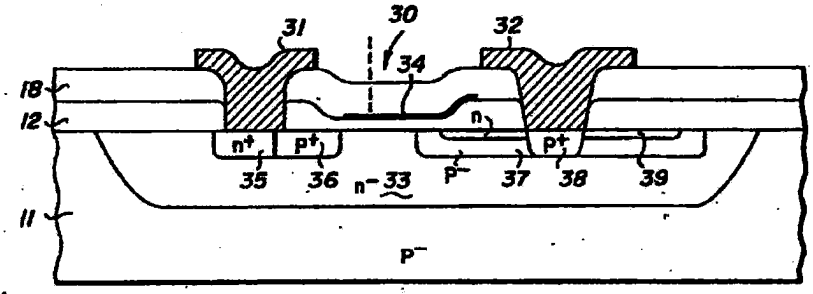

Fig_2

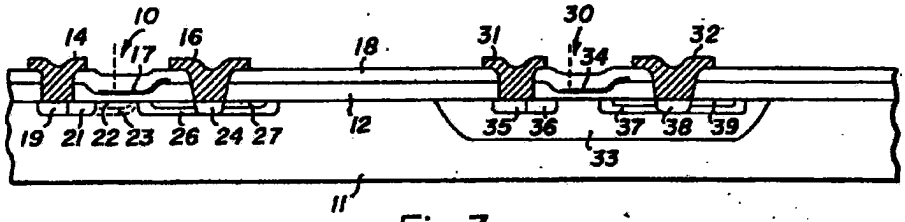

Fig_3

KLAS H. EKLUND
SS-520-01

Notice of Allowance: 08/25/88
Issue Batch No. : L66
Serial No. : 07/041,994
Filed : 04/24/87

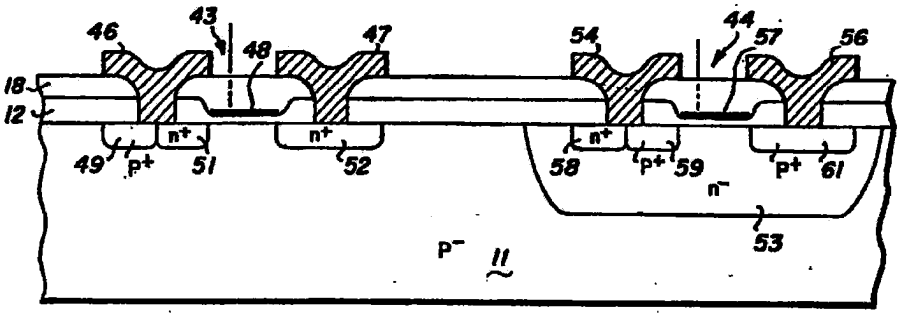

Fig_4

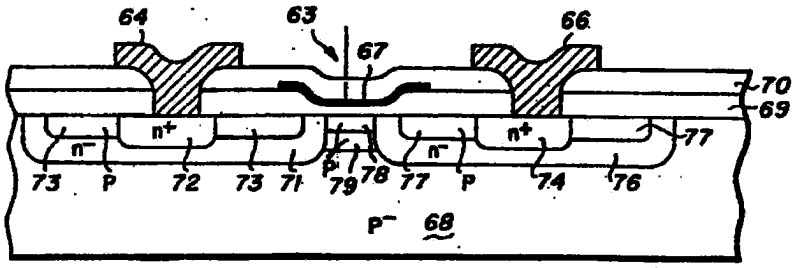

Fig_5

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eklund, Klas H. Issue Batch No.: L66

Filed : 04/24/87 Allowance Date 08/25/88

Examiner : Jackson Jr., J. Serial No. : 07/041,994

Group Art Unit : 253

Atty Docket No.: SS-520-01

For : "HIGH VOLTAGE MOS TRANSISTORS"

Box Issue Fees
COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D. C. 20231

Date of This Paper

October 19, 1988

PAYMENT OF ISSUE FEE (37 CFR 1.311)

1. Applicant hereby pays the issue fee.

2. Fee (37 CFR 1.18(a))

Application status is:

__X__ small entity- fee $ 280.00

__X__ Verified Statement attached

____ Verified Statement filed

___ other than small entity- fee $ 560.00

3. Payment of fee

__X__ Enclosed please find check 11177 for $ 302.00 *

___ Charge Deposit Account 19-0310 the sum of $ _____. A duplicate of this request is attached.

* Includes Advance Order and Assignment Recordal Fee

Respectfully submitted,

Thomas E. Schatzel
Reg. No. 22,611

Attorney for Applicant

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, CA 95054-3093
Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 10/19/88
(Date of Deposit)

Thomas E. Schatzel
(Name of applicant, assignee, or Registered Representative)

(Signature) (Date)

PTO-85b (REV. 4-88)

ISSUE FEE TRANSMITTAL

U.S. Department of Commerce
Patent and Trademark Office

This form is provided at the time of a formal transmittal and should be used for transmitting the Issue Fee. Sections 1 through 5 should be completed as appropriate.

RECEIVED IN THE OFFICE OF PATENTS AND TRADEMARKS OCT 24 1988

INVENTOR'S ADDRESS CHANGE | SC/SERIAL NO.

INVENTOR'S NAME

Street Address

City, State and ZIP Code

CO-INVENTOR'S NAME

Street Address

City, State and ZIP Code

☐ Check if additional changes are on reverse side.

MAILING INSTRUCTIONS

All further correspondence including the Issue Fee Receipt, the Patent, and advanced orders will be mailed to the address entered in section 1 on PTOL-85c, unless you direct otherwise by specifying the appropriate name and address in 1A below. (Note: See box 3 below for correspondence concerning maintenance fee payments.)

2A. The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified below.

(Signature of party in interest of record) | (Date) 10/19/88

Note: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
07/041,994	04/24/87	007	JACKSON JR, J 253	08/25/88

First Named Applicant: EKLUND, KLAS H.

TITLE OF INVENTION: HIGH VOLTAGE MOS TRANSISTORS

ATTY'S DOCKET NO.	CLASS/SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
SS-520-01	357-046.000	L66	UTILITY	YES	$280.00	11/25/88

1A. Further correspondence to be mailed to the following:

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

2B. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR, alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will print.

1 LAW OFFICES OF
2 THOMAS E. SCHATZEL
A Prof. Corporation
3

DO NOT USE THIS SPACE

040 10/28/88 041994 1 242 280.00 CK
040 10/28/88 041994 1 501 15.00 CK

3. ASSIGNMENT DATA (print or type)

A. (1) ☐ This application is NOT assigned.
(2) ☐ Assignment previously submitted to the Patent and Trademark Office.
(3) ☒ Assignment submitted herewith.

B. For Printing On The Patent: (Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data below is only appropriate when an assignment has been previously submitted to the PTO or is submitted herewith. Completion of this form is NOT a substitute for filing of an assignment as required by 37 C.F.R. 1.334).

(1) NAME OF ASSIGNEE: POWER INTEGRATIONS, INC.

(2) ADDRESS: (City & State or Country) Mountain View California 94043

(3) STATE OF INCORPORATION, IF ASSIGNEE IS A CORPORATION: California

4. The following fees are enclosed: Ck. # 11177

☒ Issue fee ☒ Advanced order ☒ Assignment recording

The following fees should be charged to deposit acc. no. 19-0310

(PTOL-85c or additional copy of PTOL-85b must be enclosed)

☐ Issue fee ☐ Assignment recording
☐ Advanced order ☒ Any additional fees due

Number of advanced order copies requested. 10
(must be for 10 or more copies)

5. All correspondence relating to maintenance fees will be addressed to the correspondence address unless a separate "Fee Address" is provided to the Patent and Trademark Office (37 C.F.R. 1.363). A "Fee Address" may be submitted by the owner of record with the payment of the issue fee or thereafter by using form PTO-1537.

TRANSMIT THIS FORM WITH FEE

PTO/SB/31 (REV 4-04)

ISSUE FEE TRANSMITTAL

U.S. Department of Commerce
Patent and Trademark Office

This form is provided in lieu of formal transmittal and should be used for transmitting the Issue Fee. Sections 1A through 4 must be completed as appropriate.

INVENTOR(S) ADDRESS CHANGE | SC/SERIAL NO.

INVENTOR'S NAME

Street Address

City, State and ZIP Code

CO INVENTOR'S NAME

Street Address

City, State and ZIP Code

☐ Check if additional changes are on reverse side.

MAILING INSTRUCTIONS

All further correspondence including the Issue Fee Receipt the Patent, and advanced orders will be mailed to the addressee entered in section 1 on PTOL-85c, unless you direct otherwise by specifying the appropriate name and address in 1A below. (Note: See box 5 below for correspondence concerning maintenance fee payments.)

2A. The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified below.

(Signature of party in interest of record) | (Date) 10/19/08

Note: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

	SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
	07/191,979	01/29/87	007	JACKSON JR., J 253	08/25/88
First Named Applicant	FILIPP,	KLAS H.			

TITLE OF INVENTION: HIGH VOLTAGE MOS TRANSISTORS

	ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
	SB-520-01	357-046.000	L66	UTILITY	YES	$280.00	11/25/88

1A. Further correspondence to be mailed to the following:

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

2B. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR, alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will printed.

1 LAW OFFICES OF
2 THOMAS E. SCHATZEL
3 A Prof. Corporation

DO NOT USE THIS SPACE

3. ASSIGNMENT DATA (print or type)

A. (1) ☐ This application is NOT assigned.
(2) ☐ Assignment previously submitted to the Patent and Trademark Office.
(3) ☒ Assignment submitted herewith.

B. For Printing On The Patent: (Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data below is only appropriate when an assignment has been previously submitted to the PTO or is submitted herewith. Completion of this form is NOT a substitute for filing of an assignment as required by 37 C.F.R. 1.334).

(1) NAME OF ASSIGNEE:
POWER INTEGRATIONS, INC.

(2) ADDRESS: (City & State or Country)
Mountain View California 94043

(3) STATE OF INCORPORATION, IF ASSIGNEE IS A CORPORATION:
California

4. The following fees are enclosed: Ck. # 11177
XX Issue fee XX Advanced order ☒ Assignment recording

The following fees should be charged to deposit acc. no. 19-0910
(PTOL-85c or additional copy of PTOL-85b must be enclosed)

☐ Issue fee ☐ Assignment recording
☐ Advanced order ☒ Any additional fees due

Number of advanced order copies requested. 10
(must be for 10 or more copies)

5. All correspondence relating to maintenance fees will be addressed to the correspondence address unless a separate "Fee Address" is provided to the Patent and Trademark Office (37 C.F.R. 1.363). A "Fee Address" may be submitted by the owner of record with the payment of the issue fee or thereafter by using form PTO-1537.

TRANSMIT THIS FORM WITH FEE

Applicant or Patentee: Klas H. Eklund
Serial or Patent No.: 07/041,994
Filed or Issued: 04/24/87
For: "HIGH VOLTAGE MOS TRANSISTORS"
Attorney's Docket No. SS-520-01

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c)) - SMALL BUSINESS CONCERN

#9

MAIL ROOM OCT 24 1988 PAT. & TRADEMARK OFF.

I hereby declare that I am

[ ] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: POWER INTEGRATIONS, INC.
ADDRESS OF CONCERN: 411 Clyde Avenue
Mountain View, CA 94043

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled "HIGH VOLTAGE MOS TRANSISTORS" by inventor(s) Klas H. Eklund described in

[ ] the specification filed herewith
[X] application serial no. 07/041,994, filed April 24, 1987.
[ ] patent no. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME N/A
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

NAME N/A
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: Klas H. Eklund
TITLE OF PERSON OTHER THAN OWNER: Vice President, Engineering
ADDRESS OF PERSON SIGNING: Power Integrations, Inc., 411 Clyde Avenue, Mountain View, California 94043
SIGNATURE _____ DATE 10/19/88

10

Atty. Docket No.: SS-510-01 #10

POWER OF ATTORNEY BY ASSIGNEE

The undersigned, as Assignee of the entire right, title, and interest in and to the subject matter which is described and claimed and for which a patent is sought on the invention entitled:

HIGH VOLTAGE MOS TRANSISTORS

the specification of which

[ ] is attached hereto;

[X] was filed on April 24, 1987 as Application Serial No. 07/041,994 and was amended on 04/11/88; 08/15/88 (if applicable);

Assignment recorded on _____ (if applicable) at Reel/Frame _____

hereby elects to control the prosecution of this application and hereby appoints the following attorneys(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office in connection therewith:

Thomas E. Schatzel Reg. No. 22,611

Address all correspondence to:

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054-3093

Address all telephone calls to Thomas E. Schatzel at telephone No. (408) 727-7077.

Assignee hereby petitions and requests that this file be closed to the inventor(s), or representative(s) thereof.

POWER INTEGRATIONS, INC.

Dated: 10/18/88

by _____
Klaus H. Eklund

Title: Vice President, Engineering

POWER INTEGRATIONS, INC.
411 Clyde Avenue
Mountain View, California 94043

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Paper No. 11

8 JAN 1989

*253 4/24/87 04,994
Klas H. Eklund
High Voltage MOS Transistors

This is in response to the communication re the Power of Attorney filed 10/24/88

assignee.

1. ☐ The power of attorney to you in this application has been revoked by the applicant.

2. ☐ In view of the notice in this application of the death of _____ his power of attorney is terminated.

3. ☒ The power of attorney to you in this application has been accepted by the Commissioner of Patents & Trademarks.

_____
For Director, Operation

4. ☐ The assignee in this application has intervened and appointed an attorney of his own selection. Further correspondence will be held with said attorney. (Rule 36, Rules of Practice.)

5. ☐ The revocation of the power of attorney to _____ has been entered and said attorney has been notified. Further correspondence will be addressed to you.

assignee

6. ☐ On _____, the applicant appointed _____ as additional attorney in this application. Further correspondence will continue to be addressed to you as specified in the new power of attorney.

assignee

7. ☐ On _____, the applicant appointed _____ as additional attorney in this application. Further correspondence will be addressed to said attorney. MPEP 403.02

8. ☐ The associate power of attorney to you in this application has been revoked by the attorney of record.

Thomas E. Schatzel

Law Offices of Thomas E. Schatzel
A Professional Corp.
[illegible] Blvd., Ste. 201
[illegible], CA 95054-3[illegible]

L. Gilbert
For Director, Operation

RETAIN THIS COPY IN THE APPLICATION FILE

Copy A

FORM PTOL-305 (REV.9/75)

Attorney Docket No.: SS-520-01 PCO

PATENT & TRADEMARK OFFICE *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT MAINTENANCE DIVISION

Patent No.: 4,811,075
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Inventor(s): Klas H. Eklund

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Box: Patent Address Change
Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Please

1. Change the address of the attorney(s) of record to:

Thomas E. Schatzel, Esq.
LAW OFFICES OF
THOMAS E. SCHATZEL
A PROFESSIONAL CORPORATION
16400 LARK AVENUE, SUITE 300
LOS GATOS, CA 95032

2. Change the correspondence address of the patent owner to:

_____

_____

_____

It is certified that the person whose signature appears below has the authority to change the correspondence address for the patent.

Date: 05/03/93

(Signature) THOMAS E. SCHATZEL

LAW OFFICES OF
THOMAS E. SCHATZEL
A PROFESSIONAL CORPORATION
16400 LARK AVENUE, SUITE 300
LOS GATOS, CA 95032

Tel. No.: (408) 358-7733

Reg. No.: 22,611
(if applicable)

☐ Inventor(s)
☐ Assignee of complete interest
☒ Attorney or agent of record

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Thomas E. Schatzel
(Name of applicant, assignee or Registered Rep.)

(Signature) (Date)

THOMAS E. SCHATZEL
16400 LARK AVENUE, STE. 300
LOS GATOS, CA 95032

(Change of Correspondence Address in Patent [12-5])